REMARKS/ARGUMENTS

§103 CLAIM REJECTIONS

Claims 1-23 were rejected under 35 USC 103(a) as being unpatentable over a paper entitled "Introduction to VHDL-A Part 2: Continuous and Mixed Continuous/Discrete Concepts" by Ernst Christen (called Christen-2 in the Office Action) in combination with Applicant's remarks about prior methods for solving simultaneous equations. Applicants respectfully submit that the prior art combination being proposed by the Examiner fails to disclose or suggest a combination of steps which are now claimed in Claim 1.

The disclosure in Christen-2 is merely a colloquial description of the requirements defined in IEEE specification 1076.1. For this reason, Christen-2 is at most cumulative to IEEE specification 1076.1. And in prior amendments, Applicants have already distinguished Claim 1 over the teachings of IEEE specification 1076.1. The Examiner's use of prior art methods for solving simultaneous equations results in a combination that is still insufficient to teach the specific combination of acts recited in Claim 1.

Specifically, Christen-2 does not disclose or suggest any details of how to implement the IEEE specification 1076.1. Moreover, Applicant's remarks in the prior amendment (called Applicants' Admission) which are relied on by the Examiner in making the rejection merely indicate that any prior art method (even Newton's method) can be used to solve a set of simultaneous equations. However, the Examiner has failed to cite a reference that bridges an **inventive gap** between these two teachings: assume one starts from statements in the language defined by IEEE specification 1076.1, then how is one to formulate the equations to be solved, and what to iterate on.

In contrast, Claim 1 is amended to explicitly require partitioning of the system variables into two sets as follows: a fixed set and a dynamic set. Each system variable in the fixed set is an unknown with a fixed association to a single equation. Each system variable in the dynamic set has a dynamic slot target variable associated with one of the slots in the system of simultaneous equations. Support for the amendment to Claim 1 is found at page 3 lines 7-8 and also at page 4 lines 32-33. Such an act of partitioning is

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nowhere disclosed or suggested in the combined teachings of Christen-2 and Applicants' Admission.

In deciding on the obviousness of Claim 1, Applicants respectfully request the Examiner to consider this claim as a whole, including additional limitations of selecting, assigning, solving and using that are present in Claim 1. Specifically, Applicants submit that even if the Examiner were to find each limitation individually in a prior art reference, that would still be insufficient because their combination does not necessarily follow. Instead, the Examiner must show some prior art motivation or suggestion to make that specific combination which is recited in Claim 1.

In this context, the Examiner is requested to carefully consider what, precisely, the Applicants have invented and are seeking to patent, and how the claims relate to and define that invention. As previously stated, **Applicants are not attempting to patent the IEEE standard**, but instead Claim 1 and its dependent claims are all directed to an inventive combination of acts to be performed (which implement the standard in some embodiments).

In evaluating the relevance of the Examiner-proposed combination to Claim 1, note that Claim 1 and its dependent claims do not cover all possible ways in which the IEEE standard explained in Christen-2 can be implemented by simultaneous equations solvers of Applicants' Admission. For example, Claim 1 explicitly requires assigning a value for the active conditional equation to a **dynamic** slot target variable at the **current** analog solution **iteration**. Therefore, if another method were to use a **static** assignment scheme, in which slot assignments are unchanged regardless of the iteration, then such a method is not covered by Claim 1. The Examiner has also not shown why a skilled artisan would not use a static assignment scheme.

Applicants further note that neither a static assignment scheme nor a dynamic assignment scheme is disclosed in Christen-2, because as noted above Christen-2 merely describes a standard and does not describe any implementations. In fact Christen-2 states that the "analog solver" is merely a concept as illustrated in the Title of this paper. The conceptual nature of this paper is further illustrated by the following remark: "Only the results that the analog solver must achieve, and not its algorithms, are characterized in the

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language definition." The Examiner appears to have seen this remark, as noted at the bottom of page 5 of the Office Action.

In view of the conceptual nature of the Christen-2 article as noted above, Applicant traverses the Examiner's position about the **inherent teachings** in Christen-2. Specifically there is no indication whatsoever about the need to generate a fixed set and a dynamic set as now recited in Claim 1. And the Examiner has not shown what, if any, evidence causes a person of skill to **necessarily conclude** that two sets of the type in Claim 1 are to be created (as noted above, why would the skilled artisan not work with just a fixed set). Moreover, there is no indication by Christen-2 that conditional equations that are active are to be selected for association with slots dynamically. Even assuming the prior art were to indicate how to identify which conditional equations are active, there is no teaching on when and for what purpose the active conditional equations are to be identified, and what is to be done with them after they are identified. Such gaps in a prior art combination which is now being proposed by the Examiner cannot be ignored.

The Examiner further cited to Christen-2's example of a bouncing ball (on page 275), stating that he is interpreting v'dot as a dynamic slot target variable associated with a slot in the system of simultaneous equations. The Examiner's interpretation is incorrect. Applicants submit that Christen-2's example has the following variables and equations:

- there are 4 unknowns: v, z, v'dot, z'dot
- there are 2 characteristic expressions in the current augmentation set. If the current augmentation set is the time domain augmentation set, these are (IEEE 12.5.6.2):
    - v'dot - derivative of v with respect to time
    - z'dot - derivative of z with respect to time
- there is 1 fixed characteristic expression in the explicit set: v - z'dot, obtained from the simple simultaneous statement z'dot == v; according to IEEE 15.1
- there is 1 dynamic characteristic expression in the explicit set. Depending on the value of the condition "v > 0.0", it is one of
    - -g - v**2*air_res - v'dot
    - -g + v**2*air_res - v'dot

Note that there is no indication by Christen-2 as to how such a system of equations is to be set up inside a computer for use by a prior art method. Specifically, there is no indication

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whatsoever as to how ***to create the input which is to be provided to a simultaneous equation solver***.

In contrast, when using the method of Claim 1 in the above example, since there are 3 fixed characteristic expressions, the fixed set of system variables has size 3, and the dynamic set has size 1. This means that there is one dynamic slot target variable, to which the active conditional equation is assigned. At each iteration, a specific equation which is to be assigned to the dynamic slot target variable is selected as recited in Claim 1. In the above example, a first equation (-g - v**2*air_res - v'dot) could be selected, if the value of v is positive in an iteration. Then if the value of v is negative in the next iteration, the second equation (-g + v**2*air_res - v'dot) could be selected. In this manner, an equation that is selected by the method of Claim 1 can change (or remain same) from iteration to iteration, depending on the value of v. Although illustrated in this particular example, please note that Claim 1 is not limited to selection based only on just a condition. Instead, selections may be made in any manner, e.g. as described in Chapter 15 of the IEEE specification 1076.1 (see the examples of "if" and "case" simultaneous statements).

As stated above, Christen-2 is silent on how to generate the input to a prior art solver. Hence, the Examiner has failed to demonstrate where in the proposed combination of Christen-2 and the prior art solver is there a teaching of the type described in the previous paragraph. Accordingly, Applicants respectfully traverse all prior art rejections which are based on the Examiner-proposed combination of Christen-2 with prior art simultaneous equations solvers.

Applicants further request the Examiner to withdraw his remarks in paragraphs 5 and 29 in the current Office Action about "simultaneous equations" being equivalent to "simultaneous statements." As previously noted this is incorrect. Incorrectness in the Examiner's position is evident from the above-described example wherein the number of characteristic expressions are not necessarily same as the number of simultaneous statements. Specifically, in the example, there are 3 simple simultaneous statements and one simultaneous "if" statement (so total of four simultaneous statements). The 3 simple simultaneous statements give rise to only two characteristic expressions as explicitly seen from the example's language, namely one which is fixed which is v-z'dot and another which is dynamic and it is one of the following two (-g - v**2*air_res - v'dot) and (-g +

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v**2*air_res - v'dot). Therefore there is no equivalence between the number of simultaneous statements and the number of simultaneous equations. Hence, there cannot be a correspondence between simultaneous statements and simultaneous equations, contrary to the Examiner's position.

In the above example, by happenstance, because of use of v'dot and z'dot in a bouncing ball model expressed in VHDL language, two additional characteristic expressions are implied in an augumentation set, namely (v'dot - derivative of v with respect to time) and (z'dot - derivative of z with respect to time). However, this does not mean that there is an equivalence between the number of simultaneous statements and the number of simultaneous equations.

Further support for the Applicants' position is provide by the following quotations from the IEEE specification 1076.1:

> IEEE 12.1 1st paragraph says:
> "The elaboration of a design hierarchy creates a collection of processes interconnected by nets and certain characteristic expressions that are an implicit consequence of the declaration and association of quantities and terminals; these characteristic expressions are said to be in the structural set of characteristic expressions. The behavior of the design can be simulated by executing the collection of processes and nets and determining the values of the quantities using the structural set of characteristic expressions, an explicit set of characteristic expressions (see 15), and an augmentation set (see 12.6.5)."
>
> IEEE 12.2.4 3rd paragraph says:
> "If a given port is a quantity port or a terminal port, the association of the formal and the actual consists of the creation of characteristic expressions."
>
> IEEE 12.6.5 defines 5 kinds of augmentation sets. Each defines a number of characteristic expressions. The second paragraph in this section includes the sentence "The current augmentation set, together with the structural set and an explicit set, is used by the analog solver to determine the values of the quantities."
>
> IEEE 15.1 1st paragraph says:
> "The evaluation of a simple simultaneous statement creates one or more characteristic expressions of an explicit set."
>
> Finally, IEEE 12.6.6 4th paragraph says:
> "The analog solver has successfully determined an analog solution point when it has determined an explicit set of characteristic expressions and a value

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for each quantity such that another determination of an explicit set will yield the same explicit set ..."

Applicants have previously established that the simultaneous equations correspond to the characteristic expressions specified in the IEEE specification 1076.1. With the above explanations it becomes clear that simultaneous statements and simultaneous equations are not equivalent, contrary to the Examiner's position.

In view of the above, Applicants believe that all claims are patentable over the prior art of record. Should the Examiner have any questions concerning this paper, the Examiner is invited to call the undersigned at (408) 982-8200, ext. 3.

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